

Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT223 (SC-73) surface mountable plastic package. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Adapters
- Battery powered applications
- Industrial automation

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{RRM}	repetitive peak reverse voltage			-	-	600	V
I _{T(AV)}	average on-state current	half sine wave; $T_{sp} \le 112 \text{ °C}$; Fig. 1		-	-	0.6	A
I _{T(RMS)}	RMS on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 2;</u> <u>Fig. 3</u>		-	-	1	A
I _{TSM}	non-repetitive peak on- state current	half sine wave; T _{j(init)} = 25 °C; t _p = 10 ms; <u>Fig. 4; Fig. 5</u>		-	-	10	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms		-	-	11	A
Tj	junction temperature		[1]	-	-	125	°C
Static charac	cteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 9</u>		-	50	200	μA
Dynamic cha	aracteristics	·					
dV _D /dt	rate of rise of off-state voltage	$\label{eq:VDM} \begin{array}{l} V_{DM} = 402 \; V; \; T_{j} = 125 \; ^{\circ}C; \; R_{GK} = 100 \; \Omega; \\ (V_{DM} = 67\% \; of \; V_{DRM}); \; exponential \\ waveform; \; \overline{Fig. 14} \end{array}$		-	50	-	V/µs

[1] Operation above 110°C may require the use of a gate to cathode resistor of $1k\Omega$ or less.

5. Pinning information

Table 2. Pinning information							
Pin	Symbol	Description	Simplified outline	Graphic symbol			
1	К	cathode	4	А - DI- К			
2	А	anode		G sym037			
3	G	gate		Symosi			
4	mb	mb; connected to anode	∐1 ∐2 ∐3 SC-73 (SOT223)				

6. Ordering information

Table 3. Ordering information						
Type number	Package					
	Name	Description	Version			
BT148W-600R	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223			

7. Limiting values

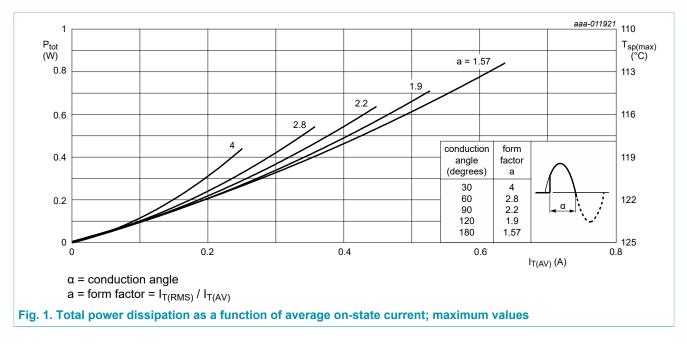
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		[1]	-	600	V
V _{RRM}	repetitive peak reverse voltage			-	600	V
I _{T(AV)}	average on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 1</u>		-	0.6	А
I _{T(RMS)}	RMS on-state current	half sine wave; T _{sp} ≤ 112 °C; <u>Fig. 2</u> ; <u>Fig. 3</u>		-	1	А
I _{TSM}	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	10	A
		half sine wave; T _{j(init)} = 25 °C; t _p = 8.3 ms		-	11	А
l ² t	I ² t for fusing	t _p = 10 ms; SIN		-	0.5	A²s
dl _T /dt	rate of rise of on-state current	I _G = 400 μA		-	100	A/µs
I _{GM}	peak gate current			-	1	А
V _{RGM}	peak reverse gate voltage			-	5	V
P _{GM}	peak gate power			-	1.2	W
P _{G(AV)}	average gate power	over any 20 ms period		-	0.12	W
T _{stg}	storage temperature			-40	150	°C
T _j	junction temperature		[2]	-	125	°C

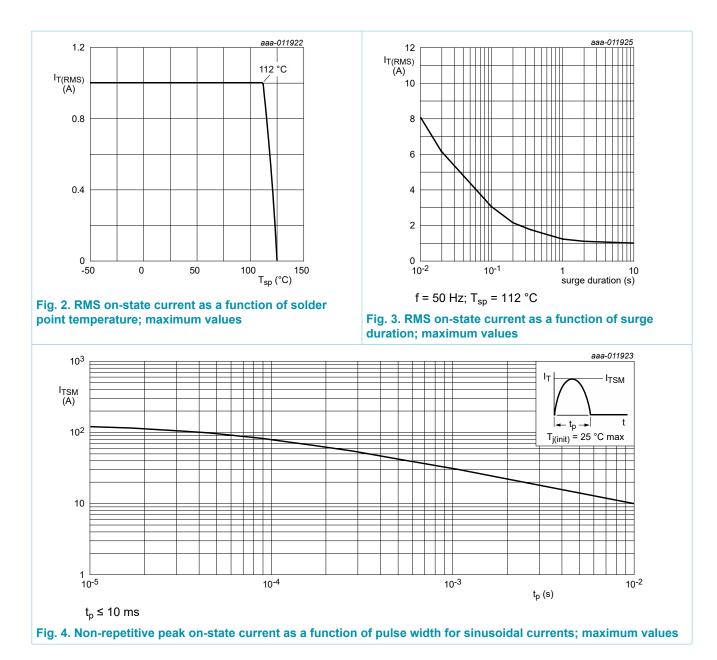
[1] Although not recommended, off-state voltages up to 800 V may be applied without damage, but the thyristor may switch to the onstate.

[2] Operation above 110°C may require the use of a gate to cathode resistor of $1k\Omega$ or less.



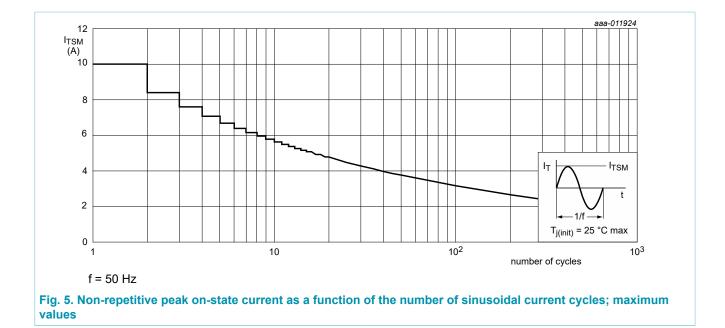
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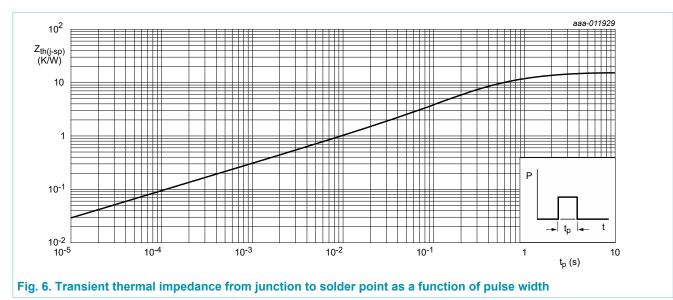
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8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-sp)}	thermal resistance from junction to solder point	<u>Fig. 6</u>	-	-	15	K/W
R _{th(j-a)}	thermal resistance from junction to	printed circuit board mounted; pad area; Fig. 7	-	70	-	K/W
	ambient free air	printed circuit board mounted; minimum footprint; Fig. 8	-	156	-	K/W

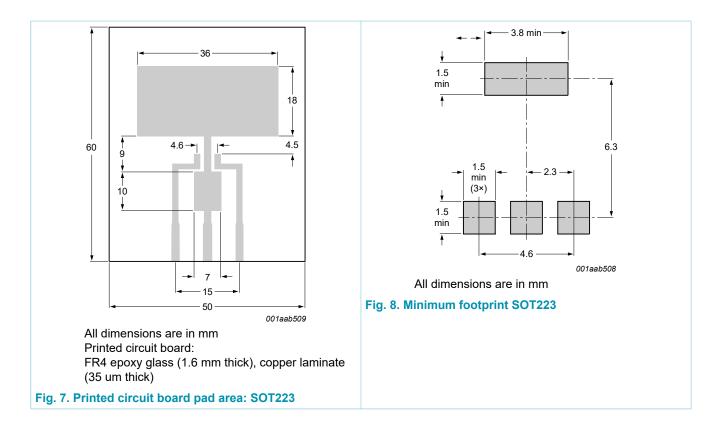


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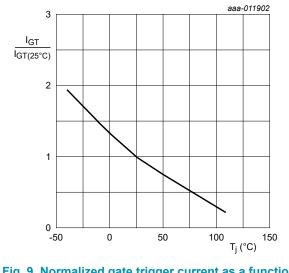
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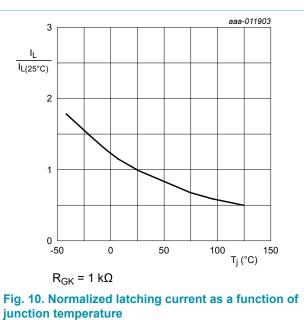


9. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		Conditions	WIIII	ТУР	IWIAA	Unit
Static chara	acteristics					_
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; <u>Fig. 9</u>	-	50	200	μA
IL	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 10		0.17	10	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 11</u>	-	0.1	6	mA
V _T	on-state voltage	I _T = 2 A; T _j = 25 °C; <u>Fig. 12</u>	-	1.3	1.5	V
V _{GT}	gate trigger voltage	V _D = 12 V; I _T = 0.1 A; T _j = 25 °C; Fig. 13	-	0.4	1	V
		$V_D = 600 \text{ V}; \text{ I}_T = 0.1 \text{ A}; \text{ T}_j = 125 \text{ °C};$ Fig. 13	0.1	0.2	-	V
I _D	off-state current	V _D = 600 V; T _j = 125 °C	-	0.1	0.5	mA
I _R	reverse current	V _R = 600 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic ch	aracteristics	· · · · ·				
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 402 V; T _j = 125 °C; R _{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM}); exponential waveform; Fig. 14	-	50	-	V/µs
t _{gt}	gate-controlled turn-on time	I_{TM} = 4 A; V _D = 600 V; I _G = 5 mA; dI _G / dt = 0.2 A/µs; T _j = 25 °C	-	2	-	μs
t _q	commutated turn-off time	$V_{DM} = 402 \text{ V}; \text{ T}_{j} = 125 \text{ °C}; \text{ I}_{TM} = 4 \text{ A};$ $V_{R} = 35 \text{ V}; (dI_{T}/dt)_{M} = 30 \text{ A}/\mu\text{s}; dV_{D}/$ $dt = 2 \text{ V}/\mu\text{s}; \text{ R}_{GK(ext)} = 1 \text{ k}\Omega; (V_{DM} = 67\% \text{ of } V_{DRM})$	-	100	-	μs

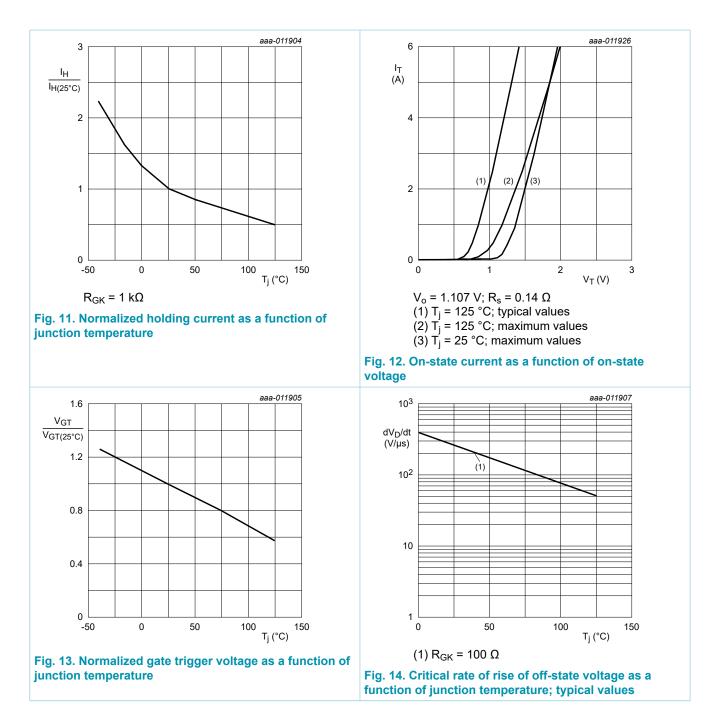






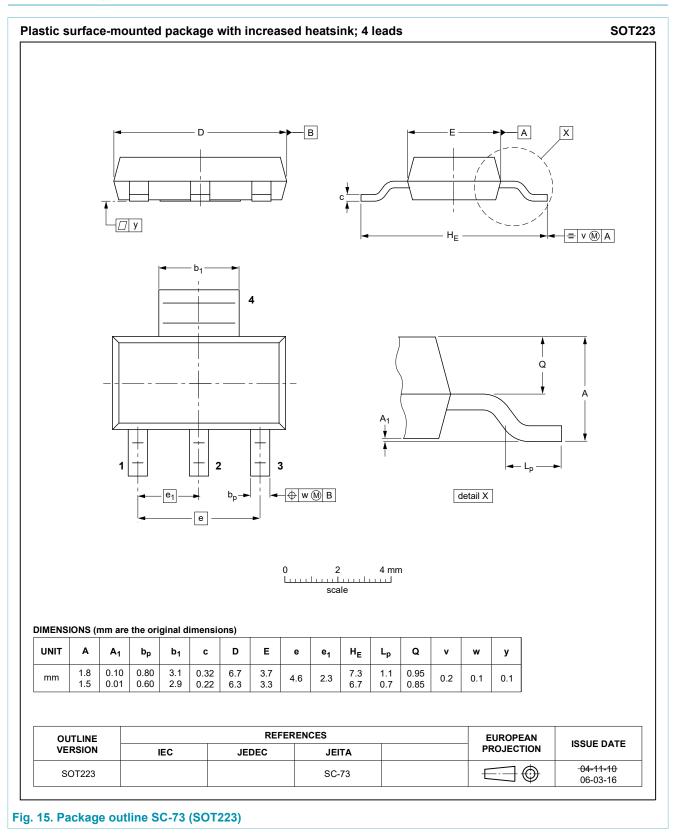
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10. Package outline



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11. Legal information

Data sheet status

Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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